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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2451	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/978,475	ROSE ET AL.	
	Examiner	Art Unit	
	KAREN C. TANG	2451	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8,10-12,14-16,24-27,30-32,34,35 and 37-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-8,10-12,14-16,24-27,30-32,34,35 and 37-43* is/are rejected.

7)☒ Claim(s) *34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

- Claims 1-4, 6-8, 10-12, 14-16, 24-27, 30-32, 34, 35, and 37-43 are presented for examination.

DETAILED ACTION

Response to Arguments

Applicant's arguments, see page 12, filed on 6/19/2009, with respect to the rejection(s) of claim(s) 1-4, 6-8, 10-12, 14-16, 24-27, 30-32, 34, 35, 37, 39-43 under 35 U.S.C 103 in view of Kano, Lay and Aimoto have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Sandoval.

Claim Objections

Claim 34 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 recites the limitation "the first point in time" in Claim 7 Lines 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 39 recites the limitation "the rate control signal" in Claim 39, Lines 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6-8, 10-12, 14-16, 24-27, 30-32, 34, 35, 37, 39-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Sandoval (US 6,990,073).

1. Referring to Claim 1, Sandoval discloses a method comprising: a transmitting device transmitting data at a first rate to a memory for storage therein during a first period of time (refer to Col 2, Lines 44); generating a first data quantity value representing a quantity of data stored in the memory at a first point in time (refer to Col 3, Lines 35), comparing a data quantity value associated with the quantity of data to a first predetermined value (refer to Col 5, Lines 20-27); comparing the first data quantity value to a first predetermined value (refer to Col 3, Lines 50-67); in response to comparing the first data quantity value to the first predetermined value, the transmitting device transmitting data at a second non-zero rate to the memory for storage therein during a second period of time (refer to Col 3, Lines 50 - Col 4, Lines 15);

modifying the first predetermined value (refer to Col 3, Lines 35-50);

wherein the second period of time is subsequent to the first period of time (refer to Col 3, Lines 35-67), and; wherein the second non-zero rate is greater than the first non-zero rate (max communication rate is greater than prior rate, refer to Col 3, Lines 35-67).

2. Referring to Claim 2. Sandoval disclosed the method of claim 1. Sandoval further disclosing the buffer used in the system is a FIFO buffer (refer to Col 2, Lines 35).

3. Referring to Claim 3. Sandoval disclosed the method of claim 1. Sandoval further disclosing wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein (refer to Col 1, Lines 45-58);

4. Referring to Claim 4. Sandoval disclosed the method of claim 1. Sandoval further disclosing: generating a rate control signal (refer to Col 2, Lines 44); and transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate (refer to 3, Lines 35-67); wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal (refer to Col 3, Lines 35-67).

5. Referring to Claim 6. Sandoval disclosed the method of claim 4. Sandoval further disclosing the comparing first data quantity value to a plurality of predetermined values (Col 3, Lines 35-Col 4, Lines 15), wherein the first predetermined value is one of the plurality of first predetermined values (refer to Col 3, Lines 35- Col 4, Lines 15); wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values (refer to Col 3, Lines 35- Col 4, Lines 15).

6. Referring to Claim 7. Sandoval disclosed the method of claim 4. Sandoval further disclosing: generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time (refer to Col 3, Lines 35- Col 4, Lines 15), wherein the second point in time is prior to the first point in time; comparing the first data quantity value to the second data quantity value (refer to Col 3, Lines 35 – Col 4, Lines 15); wherein the rate control signal is generated if comparing a data quantity associated with the first data quantity value is not equal to the second data quantity value (refer to Col 5, Lines 1-30);

7. Referring to Claim 8. Sandoval disclosed the method of claim 1. Sandoval further discloses wherein generating the first data quantity value comprises: generating total data input count at the first point in time, wherein the total data input count represents a quantity of data input to the memory device during a period of time ending in the first point in time (refer to Col 4, Lines 35 - 67); generating total data output count at the first point in time, wherein the total data output count represents a quantity of data output from the memory device during the period

of time ending in the first point in time (refer to Col 35 -67); subtracting the total output count from total data input count (refer to Col 3, Lines 59, Col 4, Lines 44);

8. Referring to Claim 10. Sandoval discloses an apparatus comprising: a memory device configured to receive data from a transmitting device for storage therein (refer to Col 2, Lines 44); a first circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate (refer to Col 3, Lines 35- Col 4, Lines 15); a second circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time (refer to Col 3, Lines 35-65); and a first comparing circuit for comparing the first data quantity value to a first predetermined value, wherein the first comparing circuit generates the rate control signal in response to comparing the first data quantity value representing a quantity of data stored in the memory with a first predetermined value (refer to Col 3, Lines 35- Col 4, Lines 15);

9. Referring to Claim 11. Sandoval disclosed the apparatus of claim 10. Sandoval further disclosing the buffer used in the system is a FIFO buffer (refer to Col 2, Lines 35).

10. Referring to Claim 12. Sandoval disclosed the apparatus of claim 10. Sandoval further disclosing wherein the transmitting device is contained in a switching fabric, wherein the memory is contained in a line card coupled to the switching fabric via a data link, and wherein

the transmitter transmits data via the data link to the memory for storage therein (refer to Col 2, Lines 45-58).

11. Referring to Claim 14. Sandoval disclosed the apparatus of claim 10. Sandoval further comprising: a plurality of comparing circuits, each one of which is configured to compare the first data quantity value to a respective one of a plurality of predetermined values (refer to Col 3, Lines 35- Col 4, Lines 15), wherein the first comparing circuit is one of the plurality of comparing circuits, and wherein the first predetermined value is one of the plurality of first predetermined values (refer to Col 3, Lines 35- Col 4, Lines 15); wherein the circuit generates the rate control signal in response to comparing the first data quantity value to the plurality of predetermined values (refer to Col 3, Lines 35- Col 4, Lines 15).

12. Referring to Claim 15. Sandoval disclosed the apparatus of claim 10. Sandoval further disclosing: a third circuit for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time, wherein the second point in time is prior to the first point in time (refer to Col 3, Lines 35- Col 4, lines 15); a second comparing circuit for comparing the first data quantity value to the second data quantity value (refer to Col 3, Lines 35 – Col 4, Lines 15); wherein the rate control signal is generated if comparing a data quantity associated with the first data quantity value is not equal to the second data quantity value (refer to Col 3, Lines 35 – Col 4, Lines 15);

13. Referring to Claim 16. Sandoval disclosed the apparatus of claim 15. Sandoval further discloses wherein the first and second circuits are the same circuits (refer to Col 3, lines 35 – Col 4, Lines 15).

14. Referring to Claim 24. Sandoval discloses an apparatus comprising: a memory device configured to receive data from a transmitting device for storage therein (refer to 2, Lines 44); a first means for generating and transmitting a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is greater than the first non-zero rate (refer to Col 3, Lines 35 – Col 4, Lines 15), a second means for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time (Col 3, Lines 35-50); a third means for comparing the first data quantity to a first predetermined value (refer to Col 3, Lines 35 – Col 4, Lines 15); wherein the first means generates the rate control signal in response to comparing the first data quantity value to the first predetermined value (refer to Col 3, Lines 35 – Col 4, Lines 15); a means for modifying the first predetermined value (refer to 3, lines 35- 50);

15. Referring to Claim 25. Sandoval disclosed the apparatus of claim 24. Sandoval further disclosing the buffer used in the system is a FIFO buffer (refer to Col 2, Lines 35).

16. Referring to Claim 26. Sandoval disclosed the apparatus of claim 24. Sandoval further disclosing wherein the transmitting device is contained in a switching fabric, wherein the

memory is contained in a line card coupled to the switching fabric via a data link, and wherein the transmitter transmits data via the data link to the memory for storage therein (refer to Col 2, Lines 45-58)

17. Referring to Claim 27. Sandoval disclosed the apparatus of claim 24. Sandoval further disclosing: a second means for generating a second data quantity value representing a quantity of data stored in the memory device at a second point in time (refer to Col 3, Lines 35- Col 4, Lines 15), wherein the second point in time is prior to the first point in time (refer to Col 3, lines 35 – Col 4, Lines 15); a third means for comparing the first data quantity to the second data quantity value (refer to Col 3, Lines 35 – Col 4, Lines 15); wherein the rate control signal is generated if comparing a data quantity associated with the first data quantity value is not equal to the second data quantity value (refer to Col 3, Lines 35 – Col 4, Lines 15);

18. Referring to Claim 30. Sandoval discloses a method comprising: a transmitting device transmitting data at a first rate to a memory for storage therein during a first period of time (refer to Col 2, Lines 44); generating a rate control signal by generating a first data quantity value representing a quantity of data stored in the memory at a first point in time (refer to Col 3, Lines 44-45), comparing the first data quantity value to a first predetermined value (refer to Col 3, Lines 35-40); in response to comparing the first data quantity value to the first predetermined value, the transmitting device transmitting data at a second non-zero rate to the memory for storage therein during a second period of time (refer to Col 3, Lines 35- Col 4, Lines 15); wherein the second period of time is subsequent to the first period of time (refer to Col 3, Lines

35 – Col 4, Lines 15), and; wherein the second non-zero rate is less than the first non-zero rate (refer to Col 3, Lines 35 – Col 4, Lines 15).

19. Referring to Claim 31. Sandoval discloses an apparatus comprising: memory device configured to receive data from a transmitting device for storage therein; a first circuit configured to generate and transmit a rate control signal instructing the transmitting device to stop transmitting data to the memory device at a first non-zero rate and to begin transmitting data to the memory device at a second non-zero rate wherein the second non-zero rate is less than the first non-zero rate (Col 3, Lines 35 – Col 4, Lines 15), a second circuit for generating a first data quantity value representing a quantity of data stored in the memory device at a first point in time (refer to Col 3, Lines 35 - 67); a first comparing circuit for comparing the first data quantity value to a first predetermined value (refer to Col 3, Lines 35 – Col 4, Lines 15); wherein the first comparing circuit generates the rate control signal in response to comparing the first data quantity value to the first predetermined value (refer to Col 3, Lines 35 – Col 4, Lines 15).

20. Referring to Claim 32. Sandoval disclosed the method of claim 30. Sandoval further disclosing transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate (refer to Col 3, Lines 35 – Col 4, Lines 15); wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal (refer to Col 3, Lines 35 – Col 4, Lines 15).

21. Referring to Claim 34. Sandoval disclosed the method of claim 33. Sandoval further disclosing comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values (refer to Col 3, Lines 35 – Col 4, Lines 15); wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values (refer to Col 3, Lines 35 – Col 4, Lines 15).

22. Referring to Claim 35. Sandoval disclosed the method of claim 1. Sandoval further disclosing transmitting the rate control signal to the transmitting device to instruct the transmitting device to stop transmitting data at the first non-zero rate and start transmitting data at the second non-zero rate (refer to Col 3, Lines 35 – Col 4, Lines 15); wherein the transmitting device stops transmitting data to the memory device at the first data rate and starts transmitting data to the memory device at the second data rate in response to the transmitting device receiving the rate control signal (refer to Col 3, Lines 35 – Col 4, Lines 15).

23. Referring to Claim 37. Sandoval disclosed the method of claim 35. Sandoval further disclosing comparing the first data quantity value to a plurality of predetermined values, wherein the first predetermined value is one of the plurality of first predetermined values (refer to Col 3, Lines 35 – Col 4, Lines 15); wherein the rate control signal is generated in response to comparing the first data quantity value to the plurality of predetermined values (refer to Col 3, Lines 35 – Col 4, Lines 15).

24. Referring to Claim 39. Sandoval disclosed the method of claim 1. Sandoval further discloses "wherein the first predetermined value is modified to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value (refer to Col 3, Lines 45-50)

25. Referring to Claim 40. Sandoval disclosed the apparatus of claim 10. Sandoval further discloses "wherein the first predetermined value is modified to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value (refer to Col 3, Lines 45-50)

26. Referring to Claim 41. Sandoval disclosed the apparatus of claim 24. Sandoval further discloses "wherein the first predetermined value is modified to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value (refer to Col 3, Lines 45-50)

27. Referring to Claim 42. Sandoval disclosed the apparatus of claim 30. Sandoval further discloses "wherein the first predetermined value is modified to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value (refer to Col 3, Lines 45-50)

28. Referring to Claim 43. Sandoval disclosed the apparatus of claim 31. Sandoval further discloses "wherein the first predetermined value is modified to avoid frequent receipt of the rate control signal due to oscillation of the quantity of the data stored within the memory device around the first predetermined value (refer to Col 3, Lines 45-50)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sandoval (US 6,990,073) in view of Kusumoto (US 2006/0233102).

29. Referring to Claim 38. Sandoval disclosed the method of claim 1. Although Sandoval disclosed the invention substantially as claimed, Sandoval did not explicitly disclosing "the transmitting device transmitting data at a third non-zero rate to the memory for storage therein during the third period of time; wherein the third period of time is subsequent to the second period of time and wherein the third non-zero rate is greater than the second non-zero rate;

Kusumoto, in analogous art, disclosing "the transmitting device transmitting data at a third non-zero rate to the memory for storage therein during the third period of time; wherein the third period of time is subsequent to the second period of time and wherein the third non-zero rate is greater than the second non-zero rate (refer to par 0085-0087);

It would have been obvious for one of ordinary skill in the art at the time the invention was made to combine the teaching of Sandoval with Kusumoto because Kusumoto's teaching of "the transmitting device transmitting data at a third non-zero rate to the memory for storage therein during the third period of time; wherein the third period of time is subsequent to the second period of time and wherein the third non-zero rate is greater than the second non-zero rate" would improve Sandoval's system by taking the QoS in the data into consideration in order to improve the method of data disposal avoidance.

Conclusion

A shortened statutory period for reply to this Office action is set to expire THREE MONTHS from the mailing date of this action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Karen C. Tang whose telephone number is (571)272-3116. The examiner can normally be reached on M-F 7 - 3.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571)272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Karen C Tang/
Patent Examiner, Art Unit 2451